Version: m2

Xilinx - Fundamentals & Design for Performance

Standard Level – 3 days

Xilinx - Fundamentals & Design for Performance incorporates the Xilinx classes, Fundamentals of FPGA Design and Designing for Performance. In addition to understanding Xilinx FPGA architecture, learning best Xilinx-design practices and the subtleties of the Xilinx design flow, this combined class will enable you to reduce system costs by creating more efficient designs targeting smaller FPGAs, or lower speed grade. In mastering the tools and design methodologies presented in this course, you will be able to shorten your development time and lower development costs.

This course uses materials developed by Xilinx for delivery by Doulos, the Authorised Training Provider for Xilinx in the UK and Ireland.

Who should attend?

Digital designers with an intermediate level working knowledge of VHDL or Verilog, who are new to Xilinx FPGAs and wish to gain the required expertise to tackle larger, faster and more demanding Xilinx designs.

Pre-requisites

It is essential for delegates to have completed the following E-Learning courses from Xilinx prior to attendance of the Doulos class. The material contained in the E-Learning courses is not covered in the Doulos class.

- **Basic FPGA Architecture: Slice and I/O Resources** (30 minute course)
- **Basic FPGA Architecture: Memory and Clocking** (30 minute course)
- **Basic FPGA Architecture: Architecture Wizard and Floorplan Editor** (30 minute course)

The E-Learning courses are available for download **free** from Xilinx.
http://www.xilinx.com/support/training/free-courses.htm#FPGA

Software Tools

- Xilinx ISE 10.1
- Synplicity Synplify Pro
- Mentor Graphics Precision RTL

Skills gained

After completing this comprehensive training, you will have the essential skills to:

- Use Xilinx Project Navigator to implement and FPGA design
- Assign pin locations with the Floorplan Editor tool
- Create DCM instantiations with the Architecture Wizard
- Read reports to determine whether design goals were met

For further information contact your local Doulos Sales Office.

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Version: m2

Xilinx - Fundamentals & Design for Performance

Standard Level – 3 days

- Use the Constraints Editor to enter basic global timing constraints
- Locate and modify implementation options
- Describe a flow for obtaining timing closure
- Describe architectural features of the Virtex™-5 FPGA
- Describe the features of the Digital Clock Manager (DCM) and Phase-Matched Clock Divider (PMCD) and how they can be used to improve performance
- Increase performance by duplicating registers and pipelining
- Write HDL code by using a style that is optimal for targeting Xilinx devices
- Describe different synthesis options and how they can improve performance
- Create and integrate cores into your design flow by using the CORE Generator™ software system
- Run behavioural simulation on an FPGA design that contains cores
- Pinpoint design bottlenecks by using the Timing Analyser reports
- Apply advanced timing constraints to meet your performance goals
- Use advanced implementation options to increase design performance

Course Outline

Fundamentals of FPGA Design (day 1)

- Xilinx Tool Flow
- **Lab 1**: Xilinx Tool Flow
- Reading Reports
- **Lab 2**: Architecture Wizard and Floorplan Editor
- **Lab 3**: Pre-Assigning I/O Pins
- Global Timing Constraints
- **Lab 4**: Global Timing Constraints
- Implementation Options
- **Lab 5**: Implementation Options
- Synchronous Design Techniques
- Closing Summary

Lab Descriptions

- **Lab 2** - Architecture Wizard and Floorplan Editor - Use the Architecture Wizard to customise a DCM and incorporate the DCM into the design. Use the Floorplan Editor to assign pin locations and implement the design.
- **Lab 3** - Pre-Assigning I/O Pins - This lab introduces the basics of making good I/O pin assignments with the Floorplan Editor. Use the SSO Analyser to avoid ground bounce and the Design Rule Checker to follow the I/O Banking Rules.
- **Lab 4** - Global Timing Constraints - Enter global timing constraints with the Xilinx Constraints Editor. Review the Post-Map Static Timing Report to verify that the timing constraints are realistic. Use the Post-Place & Route Static Timing Report to determine the delay of the longest constrained path for each timing constraint.

Xilinx - Fundamentals & Design for Performance

Standard Level – 3 days

- **Lab 5** - Implementation Options - Adjust process properties and I/O configuration options to improve the design performance.

Designing for Performance (days 2-3)

Day 2

- Review of Fundamentals of FPGA Design
- Designing with Virtex-5 FPGA Resources
- CORE Generator Software System
- **Lab 1**: CORE Generator Software System
- Designing Clock Resources
- **Lab 2**: Designing Clock Resources
- FPGA Design Techniques
- Synthesis Techniques
- **Lab 3**: Synthesis Techniques

Day 3

- Achieving Timing Closure
- **Lab 4**: Review of Global Timing Constraints
- Timing Groups and OFFSET Constraints
- Path-Specific Timing Constraints
- **Lab 5**: Achieving Timing Closure
- Advanced Implementation Options
- **Lab 6**: Designing for Performance
- Power Estimation (Optional)
- **Lab 7**: FPGA Editor Demo (Optional)
- ChipScope Pro analyser (Optional)
- **Lab 8**: ChipScope Pro analyser (Optional)
- Course Summary

Lab Descriptions

- **Lab 1** - CORE Generator Software System: Create a core, instantiate the core into VHDL or Verilog source code, and run behavioural simulation.
- **Lab 2** - Designing Clock Resources: Use the Clocking Wizard to configure the DCMs and global clock buffer resources.
- **Lab 3** - Synthesis Techniques: Experiment with different synthesis options and view the results. Versions of this lab are available for Synplicity Synplify Pro, Precision RTL, and Xilinx XST software.
- **Lab 4** - Review of Global Timing Constraints: Use the Constraints Editor to enter global timing constraints.
- **Lab 5** - Achieving Timing Closure: Review timing reports and enter path-specific timing constraints to meet performance goals.

Version: m2

Xilinx - Fundamentals & Design for Performance

Standard Level – 3 days

- **Lab 6** - Designing for Performance: Improve performance and maximise results solely with implementation options.
- **Lab 7** - FPGA Editor Demo: Use the FPGA Editor to view a design and add a probe to an internal net.
- **Lab 8** - ChipScope Pro Analyser: Add an internal logic analyser to a design to perform real-time debugging.