
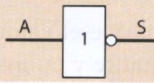
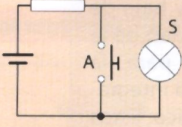
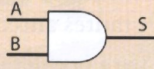
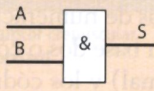
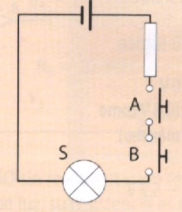

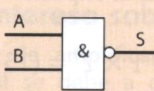
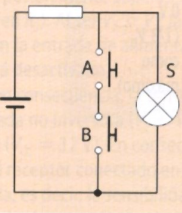
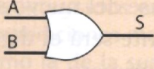
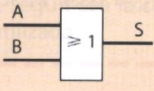
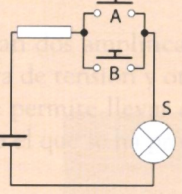
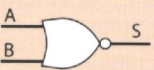
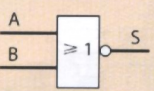
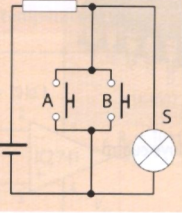
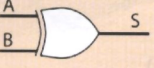
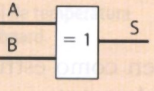
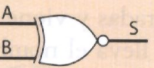
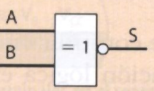


Funciones elementales

Puerta	Símbolos ASA y DIN	Función	Tabla de verdad	Configuración equivalente	Circuito integrado (TTL)															
INVERSORA (NOT)	 	Negación lógica $S = \bar{A}$	<table border="1"> <thead> <tr> <th>A</th> <th>S</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	S	0	1	1	0		7404 (6 puertas)									
A	S																			
0	1																			
1	0																			
AND	 	Producto lógico $S = A \cdot B$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>S</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	A	B	S	0	0	0	0	1	0	1	0	0	1	1	1		7408 (4 puertas de 2 entradas), 7411 (3 puertas de 3 entradas), 7421 (2 puertas de 4 entradas)
A	B	S																		
0	0	0																		
0	1	0																		
1	0	0																		
1	1	1																		
NAND	 	Función complementaria de la AND $S = \overline{A \cdot B}$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>S</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	S	0	0	1	0	1	1	1	0	1	1	1	0		7400 y 7437 (4 puertas de 2 entradas), 7410 (3 puertas de 3 entradas), 7420 y 7440 (2 puertas de 4 entradas), 7430 (1 puerta de 8 entradas)
A	B	S																		
0	0	1																		
0	1	1																		
1	0	1																		
1	1	0																		
OR	 	Suma lógica $S = A + B$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>S</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	A	B	S	0	0	0	0	1	1	1	0	1	1	1	1		7432 (4 puertas de 2 entradas)
A	B	S																		
0	0	0																		
0	1	1																		
1	0	1																		
1	1	1																		
NOR	 	Función complementaria de la OR $S = \overline{A + B}$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>S</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	S	0	0	1	0	1	0	1	0	0	1	1	0		7402 (4 puertas de 2 entradas), 7427 (3 puertas de 3 entradas), 74260 (2 puertas de 5 entradas)
A	B	S																		
0	0	1																		
0	1	0																		
1	0	0																		
1	1	0																		
OR-EXCLUSIVA (EXOR)	 	Generadora de paridad par $S = A \oplus B = \bar{A} \cdot B + A \cdot \bar{B}$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>S</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	S	0	0	0	0	1	1	1	0	1	1	1	0		7486 (4 puertas de 2 entradas)
A	B	S																		
0	0	0																		
0	1	1																		
1	0	1																		
1	1	0																		
NOR-EXCLUSIVA (EXNOR)	 	Generadora de paridad impar $S = \overline{A \oplus B} = \bar{A} \cdot \bar{B} + A \cdot B$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>S</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	A	B	S	0	0	1	0	1	0	1	0	0	1	1	1		74266 (4 puertas de 2 entradas con salidas en colector abierto)
A	B	S																		
0	0	1																		
0	1	0																		
1	0	0																		
1	1	1																		